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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/578,511	05/26/2000	Won Hyoung Park	HI-004	7993

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/578,511	PARK, WON HYOUNG	
	Examiner	Art Unit	
	Qutub Ghulamali	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-20* is/are allowed.

6)☒ Claim(s) *1,21-23,25-29,31-33,35-39,41 and 42* is/are rejected.

7)☒ Claim(s) *2-5,24,30,34 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Acknowledgment

1. This Office Action is responsive to the Amendment filed on 04/24/2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1, 22, 23, 25-29, 31-33, 35-39, 41, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Chalmers (US Patent No. 5,640,416).

Chalmers teaches (Figure 4, 5a) an Analog-to-Digital converter (406) to convert an intermediate frequency signal (416) into digital (digitized) signal (col. 4, lines 60-67) and provide a quadrature (Q) component and an in-phase (I) component of the digital signal, (col. 7, lines 41-64). A complex downconverter/polyphase filter, which receives the digitized signal and the A/D sample clock and a sample timing phase control signal, simultaneously filters and downconverts the digitized signal to baseband, corrects timing phase misalignment between the digitized signal and the locally generated pseudo-noise sequence signal, and outputs a complex corrected baseband signal (col. 18, lines 45-59), using Code Division Multiple Access (CDMA) techniques.

Regarding claims 28, 38, Chalmers teaches sampling the analog signal comprises sampling at a frequency at a rate fc of exactly four times the chip rate (col. 8, lines 18-20, col. 9, lines 52-58, col. 16, lines 63-65).

4. Claims 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Efstathiou (US Patent No. 6,504,867).

With reference to claim 21, Efstathiou teaches (Figure 1) a wideband digital radio receiver (10), which receives an analog signal and provides two channels of digitized signal (29) (Figure 2). The controller (62) provides phase shift adjustment, which receives a numerically controlled oscillator signal on lines (50, 52), a signal processor comprising of a Q channel and an I channel (44, 46) with phase controlled by a numerically controlled oscillator (49), an analog IF signal adapted to provide a CDMA formatted signal as desired (col. 1, lines 65-67), a QPSK modulated digital signal as shown in Figure 4, the matched filters include a first one-half inphase component (matched FIR filter) and a second one-half quadrature component (matched FIR filter), an input circuit to amplify (16) a filtered (11) CDMA formatted input signal and provides an intermediate frequency (24) based on amplified input signal and a second signal processor (28) to output first and second digital signals on first and second channels (Figure 2) and an output circuit to output signal having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively (Figure 4).

Allowable Subject Matter

5. Claims 2-5 and 24, 30, 34, 40, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 2-5, the following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or explicitly show; a digital sampler to sample the intermediate frequency (IF) signal, a zero-order hold device to determine an amplitude of the IF signal, a quantizer to convert the sampled IF signal processed by the zero-order hold device , a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay and, a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels, the plurality of channels comprise an In-phase channel and a Quadrature channel. Such limitations as recited in claims 2, 5, are neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest; a plurality of negators to negate the latched digital signal and output a latched signal, and a plurality of selectors coupled to each of the plurality of negators to select and output one of the negated latched signal and a unprocessed latched digital signal. Such limitations as recited in claim 3 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatters is

received by a low pass filter. Such limitations, as recited in claims 4, are neither anticipated nor rendered obvious by the prior art of record.

Regarding claims 30, 40, the following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or explicitly show, each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal is separated by three consecutive bits each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal is separated by three consecutive bits that are not associated with the in-phase component of the digital signal; each bit of said bits of the digital signal that are associated with the quadrature component of the digital signal is separated by three consecutive bits that are not associated with the quadrature component of the digital signal; and each bit of said bits of the digital signal that are associated with the in-phase component of the digital signal are adjacent a bit of said of the digital signal that is associated with the quadrature component of the digital signal.

Such limitations as recited in claims 30, 40 are neither anticipated nor rendered obvious by the prior art of record.

Regarding claims 24, 34, the prior art does not teach or fairly suggest the apparatus comprises at least one buffer; at least one latch; at least one flip-flop; and at least one formatter. Such limitations as recited in claims 24, 34, are neither anticipated nor rendered obvious by the prior art of record.

6. Claims 6-9, 10-20, are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not teach or explicitly show; a digital sampler to sample the intermediate frequency (IF) signal, a zero-order hold device to determine an amplitude of the IF signal, a quantizer to convert the sampled IF signal processed by the zero-order hold device, a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay, and a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels. Such limitations as recited in claim 6 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest; a plurality of negators to negate the latched digital signal and output a latched signal, and a plurality of selectors coupled to each of the plurality of negators to select and output one of the negated latched signal and a unprocessed latched digital signal. Such limitations as recited in claim 7 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatters is received by a low pass filter. Such limitations, as recited in claims 8, are neither anticipated nor rendered obvious by the prior art of record.

Similarly, the prior art does not teach or fairly suggest the plurality of channels comprise an In-phase channel and a Quadrature channel. Such limitations, as recited in claims 9, are neither anticipated nor rendered obvious by the prior art of record.

Regarding claim 10, the prior art does not teach or explicitly show; a signal processor, comprising: a digitizer, which receives an analog signal and generates a digital signal, wherein

the digitizer comprises: a sampler, which receives and samples the analog signal, a zero order hold circuit, which receives an output of the sampler and determines an amplitude of the received signal, and a quantizer, which receives an output of the zero order hold circuit and generates the digital signal, a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase; and a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

Such limitations as recited in claim 10 is neither anticipated nor rendered obvious by the prior art of record.

Similarly, dependent claims 11-20, recite limitations that are neither anticipated nor rendered obvious by the prior art of record.

Response to Arguments

8. Applicant's arguments filed 04/24/2003 have been fully considered but they are not persuasive. Applicant traverses the rejection by mainly arguing that the cited reference Chalmers (US Patent No. 5,640,416) fail to teach the limitations of the claimed subject matter 1. However, the examiner respectfully disagrees:

9. In response to applicant's argument that the reference A/D converter 406 in Chalmer (US Patent 5,640,416) produces an aliased spectrum and that an aliased is not a digital signal, the examiner respectfully draws applicant's attention col. 4, lines 65-67 and col. 5, lines 1-42) that clearly states that the output from the A/D converter is a digitized signal, that the digitized signal is input to the low pass digital filters (col. 4, lines 42-46). The signals (fig. 5a) 514 and 515 are

digital I and Q signals as shown in fig. 5a. Also the aliased signal as shown in fig. 6b which the applicant claims as not being digital signal is in fact shown in the frequency domain that represents a sampling of the frequency of the digitized signal. Based on the information disclosed in the reference art the examiner therefore, considers the reference cited reads on the claim making this argument mute.

Based on the above rational, it is believed that the limitations of claim 1 is met by reference to Chalmers (US Patent 5,640,416). Therefore the rejection to claim 1 is still maintained.

10. In response to applicant's argument to rejection of claim 21, as being anticipated by Efstathiou (US Patent 6,504,867). The claim recites an analog-to-digital converter to convert an intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate first and and second digital signals based on the intermediate digital signal. The examiner respectfully, likes to draw the attention of the applicant to figs 1, 2, that show an A/D converter provide a wideband digitized signal on line 29 to a plurality of tuners 30-32 (col. 3, lines 33-43), the signal on line 29 is input to signal multipliers 40-42 that provide in-phase (I) and quadrature (Q) signals on line 44, 46 respectively, to channel filters 48 (col. 3, lines 55-58). Based on the above rational, it is believed that the limitations of claim 21 is met by reference to Efstathiou (US Patent 6,504,867). Therefore the rejection to claim 21 is still maintained.

11. The rejection to claim 5 has been withdrawn because of allowance to claim 2.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (703) 305-7868. The examiner can normally be reached during normal business days Monday-Friday from 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are 703 305-3988 for regular communications and 703 305-3988 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-4750.

QG.
July 13, 2003

DON N. VO
PRIMARY EXAMINER